TECHNICAL REPORT

TR-286

Testing of Metallic Line Testing (MELT) functionality on xDSL Ports

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Issue History

Issue Number	Approval Date	Publication Date	Issue Editor	Changes
1	26 November 2012	17 December 2012	Aleksandra Kozarev, Lantiq	Original
1 Amendment 1	3 March 2014	3 April 2014	Aleksandra Kozarev, Lantiq	Next revision

Comments or questions about this Broadband Forum Technical Report should be directed to help@broadband-forum.org.

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Table of Contents

Executive Summary

See *Executive Summary/TR-286 Issue 1*.

TR-286 contains new tests or modifications to the TR-286 Issue 1 text.

The following section is added:

- Section 5.1.8 (*Combined measurement of 4-element resistance and 3-element capacitance*)

The following sections are modified:

- Section 4.5.1 (*Measurement Class (MELT-MCLASS)*)
- Section 5.1.1 (*The 4-Element DC Resistance*)
- Section 5.1.2 (*The 3-Element Capacitance*)
- Section 5.1.4 (*Loop Capacitance*)
- Section 5.1.5 (*Loop Resistance*)
- Section 5.1.6 (*The 3-Element Complex Admittance*)
- Section 5.1.7 (*Loop Complex Admittance*)

1 Purpose and Scope

See *Section 1/TR-286 Issue 1*.

2 References and Terminology

2.1 Conventions

In this Technical Report, several words are used to signify the requirements of the specification. These words are always capitalized. More information can be found be in RFC 2119 [1].

SHALL	This word, or the term “REQUIRED”, means that the definition is an absolute requirement of the specification.
SHALL NOT	This phrase means that the definition is an absolute prohibition of the specification.
SHOULD	This word, or the term “RECOMMENDED”, means that there could exist valid reasons in particular circumstances to ignore this item, but the full implications need to be understood and carefully weighed before choosing a different course.
SHOULD NOT	This phrase, or the phrase "NOT RECOMMENDED" means that there could exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications need to be understood and the case carefully weighed before implementing any behavior described with this label.
MAY	This word, or the term “OPTIONAL”, means that this item is one of an allowed set of alternatives. An implementation that does not include this option SHALL be prepared to inter-operate with another implementation that does include the option.

2.2 References

The following references are of relevance to this Technical Report. At the time of publication, the editions indicated were valid. All references are subject to revision; users of this Technical Report are therefore encouraged to investigate the possibility of applying the most recent edition of the references listed below.

A list of currently valid Broadband Forum Technical Reports is published at www.broadband-forum.org.

See *Section 2.2/TR-286 Issue 1*.

Document		Title	Source	Year
[1]	TR-286 Issue 1	*Testing of Metallic Line testing (MELT) functionality on xDSL Ports*	BBF	2012
[2]	RFC 2119	*Key words for use in RFCs to Indicate Requirement Levels*	IETF	1997

2.3 Definitions

The following terminology is used throughout this Technical Report.

See *Section 2.3/TR-286 Issue 1*.

2.4 Abbreviations

This Technical Report uses the following abbreviations:

See *Section 2.4/TR-286 Issue 1*.

3 Technical Report Impact

3.1 Energy Efficiency

TR-286 has no impact on energy efficiency.

3.2 IPv6

TR-286 has no impact on IPv6.

3.3 Security

TR-286 has no impact on security.

3.4 Privacy

Any issues regarding privacy are not affected by TR-286.

4 Combined multiple component measurement

Add section 5.1.8 Combined measurement of 4-element resistance and 3-element capacitance as follows:

5.1.8 Combined measurement of 4-element resistance and 3-element capacitance

Purpose of this test defined in Table 40 is to verify that a combined measurement performed on a multiple component test network shown in Figure 11 meet the accuracy requirements defined in Section E.1.1.12 of G.996.2 Amendment 4. The test network consists of six components located tip-to-ring, tip-to-ground and ring-to-ground, with neither foreign voltages nor a signature network connected to it. The 7-element parameter set, that is the four DC resistances (R_{TR}, R_{RT}, R_{TG} and R_{RG}) and the three capacitances (C_{TR}, C_{TG} and C_{RG}) shall be measured and reported.

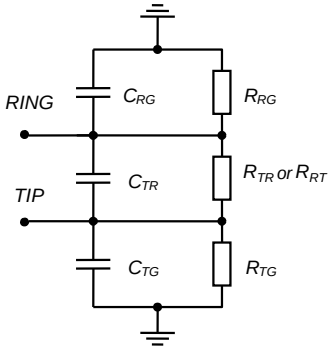

Figure 11: Multiple Component Test Network

External components for the combined measurement are defined in Table 38 for ADSL2plus and VDSL2 equipment and Table 39 for SHDSL equipment.

Table 38: External components for the combined measurement on ADSL2plus and VDSL2 equipment

Multiple Component Set 1	Component Value
Resistance *tip-to-ground* (R_{TG})	6.8 MΩ
Resistance *ring-to-ground* (R_{RG})	4.7 MΩ
Resistance *tip-to-ring* (R_{TR}, R_{RT})	1 MΩ
Capacitance *tip-to-ground* (C_{TG})	22 nF
Capacitance *ring-to-ground* (C_{RG})	47 nF
Capacitance *tip-to-ring* (C_{TR})	10 nF
Multiple Component Set 2	**Component Value**
Resistance *tip-to-ground* (R_{TG})	1 MΩ
Resistance *ring-to-ground* (R_{RG})	6.8 MΩ
Resistance *tip-to-ring* (R_{TR}, R_{RT})	4.7 MΩ
Capacitance *tip-to-ground* (C_{TG})	47 nF
Capacitance *ring-to-ground* (C_{RG})	100 nF
Capacitance *tip-to-ring* (C_{TR})	22 nF
Multiple Component Set 3	**Component Value**
Resistance *tip-to-ground* (R_{TG})	4.7 MΩ
Resistance *ring-to-ground* (R_{RG})	1 MΩ
Resistance *tip-to-ring* (R_{TR}, R_{RT})	6.8 MΩ
Capacitance *tip-to-ground* (C_{TG})	100 nF
Capacitance *ring-to-ground* (C_{RG})	470 nF
Capacitance *tip-to-ring* (C_{TR})	47 nF

Table 39: External components for the combined measurement on SHDSL equipment

Multiple Component Set 1	Component Value
Resistance *tip-to-ground* (R_{TG})	6.8 MΩ
Resistance *ring-to-ground* (R_{RG})	4.7 MΩ
Resistance *tip-to-ring* (R_{TR}, R_{RT})	1 MΩ
Capacitance *tip-to-ground* (C_{TG})	22 nF
Capacitance *ring-to-ground* (C_{RG})	47 nF
Capacitance *tip-to-ring* (C_{TR})	470 nF
Multiple Component Set 2	**Component Value**
Resistance *tip-to-ground* (R_{TG})	1 MΩ
Resistance *ring-to-ground* (R_{RG})	6.8 MΩ
Resistance *tip-to-ring* (R_{TR}, R_{RT})	4.7 MΩ
Capacitance *tip-to-ground* (C_{TG})	47 nF
Capacitance *ring-to-ground* (C_{RG})	100 nF
Capacitance *tip-to-ring* (C_{TR})	470 nF
Multiple Component Set 3	**Component Value**
Resistance *tip-to-ground* (R_{TG})	4.7 MΩ
Resistance *ring-to-ground* (R_{RG})	1 MΩ
Resistance *tip-to-ring* (R_{TR}, R_{RT})	6.8 MΩ
Capacitance *tip-to-ground* (C_{TG})	100 nF
Capacitance *ring-to-ground* (C_{RG})	470 nF
Capacitance *tip-to-ring* (C_{TR})	1 µF

Table 40: Combined multiple component measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.1 for definition of the test resistors. Each test resistor SHALL meet tolerance limits of Table 2/TR-286. (3) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3/TR-286. (4) See Table 38 and Table 39 for the definition of the multiple component sets. (5) Set the DSL port to IDLE.
Method of Procedure	(1) Apply multiple component set 1. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat steps (2) and (3) applying multiple component set 2 and 3.
Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2. (2) Measured resistance values R_{TR}, R_{RT}, R_{TG} and R_{RG} SHALL meet the accuracy limits defined in Table E.11.8/G.996.2 Amd4, after adding the multimeter tolerance values defined in Table 2/TR-286.[1] (3) Measured resistance values SHALL be reported with a granularity of 1 Ω (Section E.2.3.1/G.996.2). (4) Measured capacitance values C_{TR}, C_{TG} and C_{RG} SHALL meet the accuracy limits defined in Table E.11.9/G.996.2 Amd4 and Table E.11.10/G.996.2 Amd4 (for SHDSL, Table E.11.11/G.996.2 Amd4 and Table E.11.12/G.996.2 Amd4) after adding the multimeter tolerance values defined in Table 3/TR-286.[2] (5) Measured capacitance values SHALL be reported with a granularity of 0.1nF (Section E.2.3.4/G.996.2).

[1] For example: if the required MELT accuracy is +/- 5% and the multimeter accuracy is+/-1%, the overall required accuracy is +/-6%.
[2] For example, if the required MELT accuracy is +/-3nF and the multimeter accuracy is+/-1nF, the overall required accuracy is +/-4nF.

5 Measurement Class (MELT-MCLASS)

Modify section 4.5.1 Measurement Class (MELT-MCLASS) as follows:

4.5.1 Measurement Class (MELT-MCLASS)

Parameter MELT-MCLASS defines the list of measurements to be executed:

- The same combined measurement of the 4-element DC resistance, 3-element capacitance and foreign DC and AC voltage SHALL apply in a consecutive manner to the following test cases: 4-element DC resistance measurement (test case 5.1.1), 3-element capacitance measurement (test case 5.1.2), ~~and~~ foreign DC and AC voltage measurements (test case 5.1.3) and combined multiple component measurement (test case 5.1.8).
- A single measurement SHALL apply for the following test cases: loop capacitance (test case 5.1.4), loop resistance (test case 5.1.5), 3-element complex admittance (test case 5.1.6) and loop complex admittance (test case 5.1.7)

MELT-MCLASS setting is defined in Table 10.

Table 10: MELT-MCLASS setting

List of measurements	Range	Configuration settings
List of MELT-PMD measurement functions	single measurement or combined measurement	*test cases 5.1.4-5.1.7:* single measurement *test cases 5.1.1-5.1.3, 5.1.8:* same combined measurement of the 4-element DC resistance, 3-element capacitance, ~~and~~ foreign DC and AC voltage and combined multiple component measurement

6 MELT-PMD Test Case 5.1.1

Modify section 5.1.1 The 4-Element DC Resistance as follows:

5.1.1 The 4-Element DC Resistance

5.1.1.1 Measurement of the 4-element DC resistance with a controlled metallic voltage

Test procedure for measurement of the 4-element DC resistance with a controlled metallic voltage is defined in Table 23.

Table 23: 4-element DC resistance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.1 for definition of the test resistors. Each test resistor SHALL meet tolerance limits of Table 2. (3) See Section 5.1.1.2 for ~~accuracy requirements~~ definition of the DC test voltages and currents. (4) Set DSL port to IDLE .
Method of Procedure	(1) Connect resistor R1 of Table 2 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect resistor R1 between RING and GND. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect resistor R1 between TIP and GND. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10) Repeat step (1) to (9) using all other test resistors of Table 2 (R2, R3,..., R12). (11) Connect resistor R13 of Table 6 between RING and TIP (open loop). (12) Perform MELT measurement. (13) Record the reported results of the MELT measurement.

Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2 [5]. (2) Measured resistance values R_{TR}, R_{RT}, R_{TG} and R_{RG} SHALL meet the accuracy limits defined in Table E.1/G.996.2, after adding the multimeter tolerance values defined in Table 2.[3] (3) Measured resistance values SHALL be in the range of 0 to 10 MΩ with a granularity of 1 Ω (Section E.2.3.1/G.996.2) (NOTE1). (4) If supported, the ~~Reported~~ measured test voltage values VDC_{TR}, VDC_{RT}, VDC_{TG} and VDC_{RG} ~~SHOULD~~ SHALL meet the requirements of Section 5.1.1.2 ~~(NOTE2)~~. (5) If supported, the ~~Reported~~ measured test current values IDC_{TR}, IDC_{RT}, IDC_{TG} and IDC_{RG} ~~SHOULD~~SHALL ~~-~~meet the requirements of Section 5.1.1.2 ~~(NOTE3)~~.
NOTE1: In case of an open loop (R13) measured resistance values (R_{TR}, R_{RG} and R_{TG}) greater than 10MΩ SHALL be limited to 10MΩ. ~~NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages VDC_{TR}, VDC_{RT}, VDC_{TG} and VDC_{RG} were for further study in G.996.2.~~ ~~NOTE3: At the time of publication of TR-286 the accuracy requirements for the test currents IDC_{TR}, IDC_{RT}, IDC_{TG} and IDC_{RG} were for further study in G.996.2.~~ ~~NOTE4~~NOTE2: The testing procedure will return values for the R_{TR}, R_{RT}, R_{TG}, and R_{RG} branches even if only one branch has a test load and the others are left open. The result obtained for the branch containing the test load SHALL be compared with the test load measurement from the multimeter. The other results SHALL be ignored.	

5.1.1.2 Test voltages and currents ~~in~~ for the measurement of the 4-element DC resistance with a controlled metallic voltage

Test voltages (VDC_{TR}, VDC_{RT}, VDC_{TG} and VDC_{RG}) and test currents (IDC_{TR}, IDC_{RT}, IDC_{TG} and IDC_{RG}) for the measurement of the 4-element DC resistance are defined as follows:

- ~~SHOULD be reported within~~ The accuracy ~~limits~~ for each of the DC test voltages is defined in ~~Table 24 and Table 25~~ Table E.1.1/G.996.2 Amd.3, while the ~~. Rr~~range of valid values and granularity are defined in Section E.2.3.2/G.996.2.
- The accuracy for each of the DC test currents is defined in Table E.1.2/G.996.2 Amd.3, while the range of valid values and granularity are defined in Section E.2.3.3/G.996.2.

Reporting of the test voltage and current measurements is defined in Table E.12/G.996.2 as optional MELT-PMD function.

The ~~optional~~ voltage values are returned by the procedure and represent voltages that were present at some instant of time during the test execution. In order to compare the reported values with the actual voltages, they will have to be monitored with an oscilloscope while the test is executing. Measuring them with a multimeter will not be possible.

The ~~optional~~ current values are an estimate of the current that would be measured by two ammeters connected tip-to-ground and ring-to-ground, or by one ammeter connected tip-to-ring. They are not current values that can be measured during the test execution.

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[3] For example: if the required MELT accuracy is +/- 5% and the multimeter accuracy is+/-1%, the overall required accuracy is +/-6%.

Table 24: Test voltages in the 4-element DC resistance measurement

Test voltage (V)	Accuracy	Granularity
$-20 \leq VDC_{XY} \leq 20$	± 1 V	100mV
$-100 < VDC_{XY} < -20$ $20 < VDC_{XY} < 100$	± 5 %	100mV

Table 25: Test currents in the 4-element DC resistance measurement

Test current (mA)	Accuracy	Granularity
$-20 \leq IDC_{XY} \leq 20$	± 2 mA	1 µA
$-100 < IDC_{XY} < -20$ $20 < IDC_{XY} < 100$	± 10 %	1 µA

7 MELT-PMD Test Case 5.1.2

Modify section 5.1.2 The 3-Element Capacitance as follows:

5.1.2 The 3-Element Capacitance

5.1.2.1 Measurement of the 3-element capacitance with a controlled metallic voltage

Test procedure for measurement of the 3-element capacitance with a controlled metallic voltage is defined in Table 26.

Table 26: 3-element capacitance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.2.2 for ~~accuracy requirements~~ definition of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C1 of Table 3 between RING and TIP (open loop). (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect capacitor C2 of Table 3 between RING and TIP. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect capacitor C2 between RING and GND. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10)Connect capacitor C2 between TIP and GND. (11)Perform MELT measurement. (12)Record the reported results of the MELT measurement. (13)Repeat step (4) to (12) using all other capacitors of Table 3 (C3, C4,...,C8).

Expected Result	(1) MELT measurement SHALL be performed in less than 20 seconds, as defined in Section E.1.1/G.996.2. (2) Measured capacitance values C_{TR}, C_{TG} and C_{RG} SHALL meet the accuracy limits defined in Table E.2/G.996.2 and Table E.3/G.996.2 (for SHDSL, Table E.4/G.996.2 and Table E.5/G.996.2), after adding the multimeter tolerance values defined in Table 3.[4] (3) Measured capacitance values SHALL be in the range of 0 to 5 µF with a granularity of 0.1nF (Section E.2.3.4/G.996.2) (NOTE1). (4) If supported, the ~~Reported~~ measured test voltage values $VAC_{TR\text{-}CC}$, $VAC_{TG\text{-}CC}$ and $VAC_{RG\text{-}CC}$ and frequency ~~SHOULD~~SHALL meet the requirements of Section 5.1.2.2 ~~(NOTE2)~~.
NOTE1: In case of an open loop (C1) measured capacitance values (C_{TR}, C_{RG} and C_{TG}) SHALL be 0nF ± 3nF. Negative results may be rounded to 0nF, see Section E.2.3.4/G.996.2. ~~NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages $VAC_{TR\text{-}CC}$, $VAC_{TG\text{-}CC}$ and $VAC_{RG\text{-}CC}$ were for further study in G.996.2.~~ ~~NOTE3~~NOTE2: The testing procedure will return values for the C_{TR}, C_{TG}, and C_{RG} branches even if only one branch has a test load and the others are left open. The result obtained for the branch containing the test load SHALL be compared with the test load measured with the multimeter. The other results SHALL be ignored.	

5.1.2.1 Test voltages ~~in~~ for the 3-element capacitance test with a controlled metallic voltage

Test voltages ($VAC_{TR\text{-}CC}$, $VAC_{TG\text{-}CC}$ and $VAC_{RG\text{-}CC}$) for the measurement of the 3-element capacitance (if performed with a sinewave signal) are defined as follows:

- ~~SHOULD be reported within~~The accuracy ~~limits~~ for each of the AC voltages is defined in ~~Table 27~~Table E.11.2/ G.996.2 Amd.3, while the ~~, R~~range of valid values and granularity are defined in Section E.2.3.11/G.996.2.

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Reporting of the test voltage measurements is defined in Table E.12/G.996.2 as optional MELT-PMD function.

The ~~optional~~ voltage values are returned by the procedure and represent voltages that were present at some instant of time during the test execution. In order to compare the reported values with the actual voltages, they will have to be monitored with an oscilloscope while the test is executing. Measuring them with a multimeter will not be possible.

~~**Table 27: Test voltages in the 3-element capacitance measurement**~~

~~Test voltage (Vrms)~~	~~Accuracy~~	~~Granularity~~
~~$0 \leq VAC_{XY\text{-}CC} \leq 10$~~	~~± 0.5 Vrms~~	~~100mV~~
~~$10 < VAC_{XY\text{-}CC} < 100$~~	~~± 5 %~~	~~100mV~~

Range of valid values and granularity for the measurement frequency for a 3-element capacitance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

[4] For example, if the required MELT accuracy is +/-3nF and the multimeter accuracy is+/-1nF, the overall required accuracy is +/-4nF.

8 MELT-PMD Test Case 5.1.4

Modify section 5.1.4 Loop Capacitance as follows:

5.1.4 Loop Capacitance

5.1.4.1 Measurement of the loop capacitance with a high metallic voltage

Test procedure for measurement of loop capacitance with a high metallic voltage is defined in Table 30.

Table 30: Loop capacitance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.4.2 for ~~accuracy requirements~~ definition of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C2 of Table 3 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat steps (1) to (3) using all other capacitors of Table 3 (C3, C4,...,C8).
Expected Result	(1) The loop capacitance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured capacitance value $C_{TR,HV}$ SHALL meet the accuracy limits defined in Table E.9/G.996.2 (for SHDSL, Table E.10/G.996.2), after adding the multimeter tolerance values defined in Table 3. (3) Measured capacitance values SHALL be in the range of 0 to 5 µF with a granularity of 0.1nF (Section E.2.3.6/G.996.2). (4) If supported, the ~~Reported~~ measured test voltage value $VAC_{TR\text{-}HC}$ and frequency ~~SHOULD~~SHALL meet the requirements of Section 5.1.4.2 ~~(NOTE2)~~.
NOTE1: At the time of publication of TR-286 the maximum test time for the loop capacitance measurement was not defined in G.996.2. ~~NOTE2: At the time of publication of TR-286 the accuracy requirement for the test voltage $VAC_{TR\text{-}HC}$ was for further study in G.996.2.~~	

5.1.4.2 Test voltage ~~in~~ for the loop capacitance test with a high metallic voltage

Test voltage ($VAC_{TR\text{-}HC}$) for the measurement of the loop capacitance (if performed with a sinewave signal) is defined as follows:

- ~~SHOULD be reported within~~ The accuracy ~~limits~~ of this parameter defined in ~~Table 31~~ Table E.11.3/G.996.2 Amd.3, while the ~~. R~~range of valid values and granularity are defined in Section E.2.3.12/G.996.2.

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Reporting of the test voltage measurements is defined in Table E.12/G.996.2 as optional MELT-PMD function.

This ~~optional~~ voltage value is returned by the procedure and represents a voltage that was present at some instant of time during the test execution. In order to compare the reported value with the actual voltage, it will have to be monitored with an oscilloscope at the same time the test is executing. Measuring it with a multimeter will not be possible.

~~**Table 31: Test voltages in the loop capacitance measurement**~~

~~**Test voltage (Vrms)**~~	~~**Accuracy**~~	~~**Granularity**~~
~~$0 \leq VAC_{TR\text{-}HC} \leq 10$~~	~~± 0.5 Vrms~~	~~100mV~~
~~$10 < VAC_{TR\text{-}HC} < 100$~~	~~± 5 %~~	~~100mV~~

Range of valid values and granularity for the measurement frequency for the loop capacitance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

9 MELT-PMD Test Case 5.1.5

Modify section 5.1.5 Loop Resistance as follows:

5.1.5 Loop Resistance

5.1.5.1 Measurement of the loop resistance with a high metallic voltage

Test procedure for measurement of loop resistance with a high metallic voltage is defined in Table 32.

Table 32: Loop resistance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.1 for definition of the test resistors. Each test resistor SHALL meet tolerance limits of Table 2. (3) See Section 5.1.5.2 for ~~accuracy requirements~~ definition of the DC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect resistor R2 of Table 2 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat step (1) to (3) using the following resistors of Table 2: R3, R4, R5, R6, R7 and R8.
Expected Result	(1) The loop resistance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured resistance values $R_{TR,HV}$ and $R_{RT,HV}$ SHALL meet the accuracy limits defined in Table E.11/G.996.2, after adding the multimeter tolerance values defined in Table 2. (3) Measured resistance values SHALL be in the range of 0 to 10 MΩ with a granularity of 1 Ω (Section E.2.3.7/G.996.2). (4) If supported, the ~~Reported~~measured test voltage values $VDCH_{TR}$ and $VDCH_{RT}$ ~~SHOULD~~SHALL meet the requirements of Section 5.1.5.2 ~~(NOTE2)~~.
NOTE1: At the time of publication of TR-286 the maximum test time for the loop resistance measurement was not defined in G.996.2. ~~NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages $VDCH_{TR}$ and $VDCH_{RT}$ were for further study in G.996.2.~~	

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5.1.5.2 Test voltage in the measurement of the loop resistance with high metallic voltage

Test voltages ($VDCH_{TR}$ and $VDCH_{RT}$) for the measurement of the loop resistance are defined as follows:

- ~~SHOULD be reported within~~ The accuracy ~~limits~~ for each of the test voltages is defined in ~~Table 33~~ Table E.11.1/G.996.2 Amd.3, while the ~~. R~~range of valid values and granularity are defined in Section E.2.3.8/G.996.2.

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Reporting of the test voltage measurements is defined in Table E.12/G.996.2 as optional MELT-PMD function.

This ~~optional~~ voltage value~~s is~~ are returned by the procedure and represents a voltage that was present at some instant of time during the test execution. In order to compare the reported value with the actual voltage, it will have to be monitored with an oscilloscope at the same time the test is executing. Measuring it with a multimeter will not be possible.

~~**Table 33: Test voltages in the loop resistance measurement**~~

~~**Test voltage (V)**~~	~~**Accuracy**~~	~~**Granularity**~~
~~$-20 \leq VDCH_{XY} \leq 20$~~	~~± 1 V~~	~~100mV~~
~~$-100 < VDCH_{XY} < -20$~~ ~~$20 < VDCH_{XY} < 100$~~	~~± 5 %~~	~~100mV~~

10 MELT-PMD Test Case 5.1.6

Modify section 5.1.6 The 3-Element complex admittance as follows:

5.1.6 The 3-Element complex admittance

5.1.6.1 Measurement of the 3-element complex admittances with a controlled metallic voltage

The complex admittance Y_{XY} ($Y_{XY} = abs(G_{XY} + jB_{XY})$) MAY be automatically provided by the 3-element capacitance measurement with controlled metallic voltage defined in Section 5.1.2. Alternatively, the test procedure defined in Table 34 SHOULD apply.

Table 34: 3-element complex admittance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.6.2 for ~~accuracy requirements~~ definition of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C1 of Table 3 between RING and TIP (open loop). (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Connect capacitor C2 of Table 3 between RING and TIP. (5) Perform MELT measurement. (6) Record the reported results of the MELT measurement. (7) Connect capacitor C2 between RING and GND. (8) Perform MELT measurement. (9) Record the reported results of the MELT measurement. (10)Connect capacitor C2 between TIP and GND. (11)Perform MELT measurement. (12)Record the reported results of the MELT measurement. (13)Repeat step (4) to (12) using all other capacitors of Table 3 (C3, C4,...,C8).
Expected Result	(1) The 3-element complex admittance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured admittance values (G_{TR}, B_{TR}, G_{TG}, B_{TG}, G_{RG} and B_{RG}) SHALL be in the range of 0.1 µSiemens to 0.1 Siemens with a granularity of 0.1 µSiemens (Section E.2.3.9/G.996.2). (3) If supported, the ~~Reported~~ measured test voltage values VAC_{TR-CA}, VAC_{TG-CA} and VAC_{RG-CA} and frequency ~~SHOULD~~SHALL meet the requirements of Section 5.1.6.2 ~~(NOTE2)~~.

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NOTE1: At the time of publication of TR-286 the maximum test time for the 3-element complex admittance measurement was not defined in G.996.2.

~~NOTE2: At the time of publication of TR-286 the accuracy requirements for the test voltages VAC_{TR-CA}, VAC_{TG-CA} and VAC_{RG-CA} were for further study in G.996.2.~~

5.1.6.2 Test voltages ~~in~~ for the 3-element complex admittance test with a controlled metallic voltage

Test voltages (VAC_{TR-CA}, VAC_{TG-CA} and VAC_{RG-CA}) for the measurement of the 3-element complex capacitance (if performed with a sinewave signal) are defined as follows:

- ~~SHOULD be reported within~~ The accuracy ~~limits~~ for each of the test voltages is defined in ~~Table 35~~ Table E.11.4/G.996.2 Amd.2, while the ~~. R~~range of valid values and granularity are defined in Section E.2.3.13/G.996.2.

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Reporting of the test voltage measurements is defined in Table E.12/G.996.2 as optional MELT-PMD function.

These ~~optional~~ voltage values are returned by the procedure and represent voltages that were present at some instant of time during the test execution. In order to compare the reported values with the actual voltages, they will have to be monitored with an oscilloscope at the same time the test is executing. Measuring them with a multimeter will not be possible.

~~**Table 35: Test voltages in the 3-element complex capacitance measurement**~~

~~Test voltage (Vrms)~~	~~Accuracy~~	~~Granularity~~
~~$0 \leq VAC_{XY-CA} \leq 10$~~	~~± 0.5 Vrms~~	~~100mV~~
~~$10 < VAC_{XY-CA} < 100$~~	~~± 5 %~~	~~100mV~~

Range of valid values and granularity for the measurement frequency for the 3-element complex admittance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

11 MELT-PMD Test Case 5.1.7

Modify section 5.1.7 Loop complex admittance as follows:

5.1.7 Loop complex admittance

5.1.7.1 Measurement of the loop complex admittance with a high metallic voltage

Test procedure for measurement of the loop complex admittance with a high metallic voltage is defined in Table 36.

Table 36: Loop complex admittance measurement

Test Configuration	(1) See Figure 1 for the test setup. (2) See Section 4.4.2 for definition of the test capacitors. Each test capacitor SHALL meet tolerance limits of Table 3. (3) See Section 5.1.7.2 for ~~accuracy requirements~~ definition of the AC test voltages. (4) Set DSL port to IDLE.
Method of Procedure	(1) Connect capacitor C4 of Table 3 between RING and TIP. (2) Perform MELT measurement. (3) Record the reported results of the MELT measurement. (4) Repeat step (1) to (3) using the following test capacitors C5, C6 and C7 of Table 3.
Expected Result	(1) The loop complex admittance measurement SHOULD be performed in less than 20 seconds (NOTE1). (2) Measured admittance values ($G_{TR,HV}$ and $B_{TR,HV}$) SHALL be in the range of 0.1 µSiemens to 0.1 Siemens with a granularity of 0.1 µSiemens (Section E.2.3.10/G.996.2). (3) If supported, the ~~Reported~~ measured test voltage value $VAC_{TR\text{-}HA}$ and frequency ~~SHOULD~~ SHALL meet the requirements of Section 5.1.7.2 ~~(NOTE2)~~.
NOTE1: At the time of publication of TR-286 the maximum test time for the loop complex admittance measurement was not defined in G.996.2. ~~NOTE2: At the time of publication of TR-286 the accuracy requirement for the test voltage $VAC_{HR\text{-}CA}$ was for further study in G.996.2.~~	

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5.1.7.2 Test voltage ~~in~~ for the loop complex admittance test with a high metallic voltage

Test voltage ($VAC_{TR\text{-}HA}$) for the measurement of the loop complex admittance (if performed with a sinewave signal) is defined as follows:

- ~~SHOULD be reported within~~ The accuracy ~~limits~~ for this parameter is defined in ~~Table 37~~ Table E.11.5/G.996.2/Amd.3, while the the ~~. R~~range of valid values and granularity are defined in Section E.2.3.14/G.996.2.

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Reporting of the test voltage measurements is defined in Table E.12/G.996.2 as optional MELT-PMD function.

The~~is optional~~ voltage value is returned by the procedure and represents a voltage that was present at some instant of time during the test execution. In order to compare the reported value with the actual voltage, it will have to be monitored with an oscilloscope at the same time the test is executing. Measuring it with a multimeter will not be possible.

~~**Table 37: Test voltages in the loop complex admittance measurement**~~

~~**Test voltage (Vrms)**~~	~~**Accuracy**~~	~~**Granularity**~~
~~$0 \leq VAC_{TR\text{-}HA} \leq 10$~~	~~± 0.5 Vrms~~	~~100mV~~
~~$10 < VAC_{TR\text{-}HA} < 100$~~	~~± 5 %~~	~~100mV~~

Range of valid values and granularity for the measurement frequency for the loop complex admittance measurement, if performed with a sinewave signal, is from 10 to 1000Hz with a granularity of 1Hz, as defined in Section E.2.2.1/G.996.2.

End of Broadband Forum Technical Report TR-286